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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,200	10/21/2003	Salman Akram	4244.5US (97-1355.05/US)	3680

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EXAMINER	
DOLAN, JENNIFER M	
ART UNIT	PAPER NUMBER
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,200	AKRAM ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the Amendment filed 3 November 2006

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 6-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 6 recites a structure including a dielectric layer and a gate structure overlying the dielectric layer, the gate structure including a gate oxide, a polysilicon layer, a metal silicide layer, and a dielectric cap stacked on the dielectric layer, wherein the gate structure including the gate oxide, polysilicon layer, metal silicide, and dielectric cap are patterned to have sidewalls. The specification does not provide any disclosure or even a suggestion that the gate stack itself would include the gate oxide layer (i.e., the gate oxide layer is patterned to have sidewalls). Instead, the specification clearly discloses a multilayer gate dielectric layer, such as the ONO layer in paragraph 0027, wherein the "gate oxide layer" is part of the blanket deposited dielectric layer and not part of the gate structure having sidewalls.

For the purpose of examination, it is assumed that the dielectric layer (of line 2) is a multilayer including a first dielectric layer and an oxide layer disposed thereon; and that the gate structure patterned to include sidewalls does not include a gate oxide layer, such that claim 6 is consistent with the disclosure as originally filed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,866,460 to Akram et al. (cited by Applicant) in view of U.S. Patent No. 5,739,066 to Pan.

Akram discloses a method of making a transistor on a substrate (10) having a dielectric layer (14) thereon, the dielectric layer including a first dielectric layer (SiN layer of ONO in column 4, lines 8-22) and an overlying "gate oxide layer" (upper SiO layer in ONO stack), the method comprising: forming a gate structure (20,22,24; see figures 2A, 3A) overlying the dielectric layer, the gate structure including a polysilicon (20)-metal silicide (22)-dielectric (24) stack, the gate structure having first and second sidewalls (see figure 3A), defining a first contact region (region to the left of gate structure including regions 16,40, and 34), a second contact region (region to the right of gate structure including regions 16,40,34) and a channel region therebetween; and forming first (16), second (40), and third (34) subregions within the contact regions (see figures 3A-3C), each subregion having a different doping concentration from the

other subregions (see column 6, lines 17-35), wherein forming the subregions comprises the steps of: introducing a first dopant into the substrate to form the first subregion (16), the first subregion generally aligned with the sidewalls of the gate structure (figure 3A; column 7, lines 40-45); forming a single layer sidewall spacer (26) overlying the sidewalls, the single layer sidewall spacer having a relatively large thickness of 150-2000 angstroms (column 5, line 60-column 6,line 10); introducing a second dopant into the substrate to form the second subregion (40), the second subregion generally aligned with the second single layer sidewall spacer (figure 3B); reducing the thickness of the single layer sidewall spacer to form a sidewall spacer having a thickness reduced from that of the single layer sidewall spacer (see column 7, lines 20-35; figure 3C); maintaining the sidewall spacer (column 7, lines 40-45; figure 3d) and introducing a third dopant into the substrate to form the third subregion (34), the third subregion generally aligned with the third sidewall spacer (figure 3C).

Akram fails to teach formation of the first single layer sidewall spacer of a thin conformal layer of dielectric material.

Pan teaches that it is advantageous when forming a stacked gate structure substantially similar to that in Akram (see Pan, column 3, lines 1-20; figures 1-4) to include a first thin layer sidewall spacer (34,36) formed of silicon nitride (column 3, lines 20-27) overlying the gate sidewalls (figure 3), the first single thin layer sidewall spacer being formed by depositing a thin conformal layer of dielectric material (32) over the substrate (figure 2) and etching to a predetermined thickness over the sidewalls (column 3, lines 20-40; column 4, lines 39-40; note that the post-etched thickness must be less than the deposited thickness of 50-500 angstroms); and providing an annealing/oxidation step at an elevated temperature (column 3, lines 40-67).

The first thin layer sidewall spacer is disposed underneath additional sidewall spacer layers (see figures 5 and 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the thin conformal sidewall spacer and methods of forming such a layer, as taught by Pan, in the transistor formation method of Akram. The rationale is as follows: A person having ordinary skill in the art would have been motivated to include the conformal spacer underlying the additional spacers of Akram, because Pan illustrates that formation of a thin sidewall spacer followed by an annealing/oxidation step helps repair damage to the gate dielectric layer resulting from the gate stack etching and helps oxidize the portions of the polysilicon gate layer interfacing the gate dielectric layer, thus reducing hot electron degradation (see Pan, column 1, lines 25-45; column 3, line 40 – column 4, line 10). The Examiner notes that since the first sidewall spacer is disclosed as preferably 100 angstroms and as low as 50 angstroms, it is expected to be etched to a thickness between 50-150 angstroms (Pan, column 3, lines 20-40; column 4, lines 39-40), and since the second spacer is disclosed as 150-2000 angstroms, thus overlapping the claimed 550 angstroms (Akram, column 5, line 60-column 6,line 10), these conditions are generally consistent with the claimed 2 to 20 times the thickness of the first layer. Although neither Akram nor Pan provides an exact value for the spacer thicknesses, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

Response to Arguments

5. Applicant's arguments filed 3 November 2006 have been fully considered but they are not persuasive.

The Applicant first argues that the 35 U.S.C. §112 rejection has been overcome through amendment and cites paragraph 0027 of the specification as the basis for the gate oxide layer disposed on the dielectric layer. The Examiner, however, maintains that claiming that the gate oxide is part of the gate structure, and that the gate structure is patterned to have a sidewall suggests that the gate oxide is patterned to have a sidewall. Paragraph 0027 indicates that the gate dielectric material may include a multilayer structure, such as ONO. The specification and drawings indicate that the multilayer dielectric layer is blanket deposited across the substrate and is not patterned to have a sidewall on the uppermost oxide layer in the multilayer gate dielectric stack. Thus, claim 6 sets forth a structure not described in the application as originally filed.

The Examiner recommends amending claim 6 such that in line 2, "dielectric layer" is replaced by –multilayer dielectric structure wherein the top layer is an oxide—and omitting the gate oxide layer in lines 3-4.

The Applicant further argues that any combination of Akram and Pan merely uses hindsight reasoning to arrive at the claimed invention. This is not persuasive, because Akram only lacks a teaching of forming a conformal dielectric layer over the gate stack and under the sidewall spacer layer. Since Pan teaches that it is desirable to provide a conformal dielectric layer over the gate stack in order to protect the gate stack from subsequent processing steps or

undesired oxidation (see Pan, column 3, lines 20-67), the Examiner maintains that a combination of Akram and Pan is reasonable.

The Applicant further argues that neither Akram nor Pan disclose a method wherein the third sidewall spacer is maintained on the sidewall of the gate. The Examiner, however, notes that figure 3(d) and column 7, lines 40-45 of Akram indicate that a portion the sidewall spacer 26 is maintained on the sidewall.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

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